Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for arbitrating between a plurality of access requests issued in relation to a resource by a plurality of requestors in an integrated circuit, wherein each request can be one of a CPU ~~memory~~ write request from a CPU requester, a non-CPU ~~memory~~ write request from a non-CPU requester and a non-CPU ~~memory~~ read request from a non-CPU requester~~, non-CPU write request having a higher latency associated with its performance than the non-CPU read request and CPU write request~~, the method including the steps of:

(a) receiving, in a timeslot arbitrator of the integrated circuit, a plurality of the access requests;

(b) maintaining, in the timeslot arbitrator, a current pointer that points to a current timeslot in a timeslot list, and at least one lookahead pointer that points to a future timeslot in the timeslot list; and

(c) in the event an access request as arbitrated via the lookahead pointer is a non-CPU write request, initiating performance of the access request, in the timeslot arbitrator, earlier than the position in the list suggests it would be performed should it be started when the current pointer reached the timeslot,

wherein, in step (c), the earlier position is selected so as to not be adjacent a position in the list for performance of another non-CPU write request, and

each timeslot is configured to enable performance of a CPU write request then either a non-CPU write request or non-CPU read request in that timeslot.

2. (Original) A method according to claim 1, wherein step (c) includes the substep of performing the access request indicated by the lookahead pointer immediately after the access request indicated by the current pointer is performed.

3. (Currently Amended) A method according to claim 1, wherein ~~the CPU write request has a lower latency associated with its performance than the non-CPU read request,~~ step (c) ~~including~~ includes the timeslot arbitrator arbitrating in the timeslot list CPU write requests to be interleaved with non-CPU write and read requests.

4. (Previously Presented) A method according to claim 3, wherein step (c) includes the substep of performing the access request indicated by the lookahead pointer immediately after the access request indicated by the current pointer is performed.

5. (Previously Presented) A method according to claim 1, wherein the number of timeslots between the timeslot indicated by the lookahead pointer and the timeslot indicated by the current pointer takes into account a latency difference between performing the access requests.

6. (Currently Amended) An integrated circuit including:

a plurality of operative units, each of which is capable of issuing a request for access to a memory accessible by the integrated circuit including a CPU ~~memory~~ write request from a CPU requester, a non-CPU ~~memory~~ write request from a non-CPU requester and a non-CPU ~~memory~~ read request from a non-CPU requester; and

an timeslot arbitrator for arbitrating between requests issued by the operative units for access to the memory~~, the non-CPU write request having a higher latency associated with its performance than the non-CPU read request and CPU write request~~, the timeslot arbitrator being configured to:

(a) receive a plurality of the access requests;

(b) maintain a current pointer that points to a current timeslot in a timeslot list, and at least one lookahead pointer that points to a future timeslot in the timeslot list; and

(c) in the event the access request as arbitrated via the lookahead pointer is a non-CPU write request, performing the access request earlier than the position in the list suggests it should be performed should it be started when the current pointer reached the timeslot,

wherein, in (c), the earlier position is selected so as to not be adjacent a position in the list for performance of another non-CPU write request, and

each timeslot is configured to enable performance of a CPU write request then either a non-CPU write request or non-CPU read request in that timeslot.

7. (Currently Amended) An integrated circuit according to claim 6, wherein ~~the CPU write request has a lower latency associated with its performance than the non-CPU read request, and~~ in (c) the timeslot arbitrator arbitrates, in the timeslot list, CPU write requests to be interleaved with non-CPU write and read requests.

8. (Cancelled)

9. (Previously Presented) An integrated circuit according to claim 6, wherein the number of timeslots between the timeslot indicated by the lookahead pointer and the timeslot indicated by the current pointer takes into account a latency difference between performing the access requests.

10-18. (Cancelled)